

**WHAT IS CLAIMED IS:**

1. A thin film transistor array panel comprising:
  - a substrate;
  - a gate electrode;
  - 5 a gate insulating layer formed on the gate electrode;
  - a polysilicon layer formed on the gate insulating layer and including a pair of ohmic contact areas doped with conductive impurity;
  - source and drain electrodes formed on the ohmic contact areas at least in part;
  - a passivation layer formed on the source and the drain electrodes and having a
  - 10 contact hole exposing the drain electrode at least in part; and
  - a pixel electrode formed on the passivation layer and connected to the drain electrode through the contact hole.
2. The thin film transistor array panel of claim 1, wherein the conductive
- 15 impurity comprises boron or phosphorous.
3. The thin film transistor array panel of claim 1, wherein concentration of the impurity ranges from about  $1 \times 10^{14}$  to about  $1 \times 10^{16}$ .
- 20 4. The thin film transistor array panel of claim 1, further comprising:
  - a gate line disposed between the substrate and the gate insulating layer and connected to the gate electrode; and

a data line disposed between the gate insulating layer and the passivation layer and connected to the source electrode.

5        5.        A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate electrode;

depositing a gate insulating layer and a polysilicon layer on the gate electrode in sequence;

10        forming a photoresist having a first portion and a second portion thinner than the first portion on the polysilicon layer;

patterning the polysilicon layer using the photoresist as a mask to form a semiconductor layer;

removing the second portion of the photoresist;

15        performing impurity implantation using the first portion of the photoresist as a mask to form ohmic contact areas in the semiconductor layer;

removing the first portion of the photoresist;

forming source and drain electrodes on the ohmic contact areas;

forming a passivation layer having a contact hole on the drain electrode; and

forming a pixel electrode on the passivation layer.

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6.        The method of claim 5, wherein the formation of the photoresist comprising:

coating a photoresist film on the polysilicon layer;

exposing the photoresist film through a photo-mask having a slit pattern or a translucent portion facing the second portion of the photoresist; and  
developing the photoresist film to form the photoresist.

- 5            7.    The method of claim 5, wherein the impurity comprises p type conductive impurity.